

10070 U.S. PTO
09/961264

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438	239	Class	Subclass	ISSUE CLASSIFICATION
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PATENT NUMBER

U.S. UTILITY Patent Application

SCANNED <i>LM3</i>	I.P.E.	PATENT DATE
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APPLICATION NO. 09/961264	CONT/PRIOR D F	CLASS 257/438	SUBCLASS 239	ART UNIT 2871 2823	EXAMINER DAORC W. Fahmy
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APPLICANTS
Narumi Ohkawa

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TITLE
Semiconductor device having both memory and logic circuit and its manufacture

PTO-2040
1289

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
438	239	438	241	252	587	598		
INTERNATIONAL CLASSIFICATION								
H01L	21/8242							

<input type="checkbox"/> TERMINAL DISCLAIMER <input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____ <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	DRAWINGS Sheets Draw. <i>12</i> Figs. Draw. <i>27</i> Print Figs. <i>1a-1c</i>			CLAIMS ALLOWED Total Claims <i>10</i> Pending Claims <i>4</i>	
	(Accident Exemption) _____ (Date) _____ Trung Dang Primary Examiner <i>Trung Dang</i> <i>2/24/03</i> (Priority Exemption) _____ (Date) _____			NOTICE OF ALLOWANCE MAILED	
	(Legal Instruments Examiner) _____ (Date) _____			ISSUE FEE Amount Due _____ Date Paid _____	
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